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EXAMINER

MEMULA, SURESH

ART UNIT	PAPER NUMBER
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2825

DATE MAILED: 08/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/759,867	Applicant(s) GEDAMU, ELIAS	
	Examiner Suresh Memula	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 June 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This FINAL office action is a response to the amendments and remarks filed on 06/12/2006. The remarks are not persuasive; therefore, the rejections based on the prior art of record Ando is maintained.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
2. **Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
3. Regarding Claims 1, 6, 11, and 15, "evaluating a processor design"; as recited in the preambles of independent Claims 1, 6, 11, and 15; is not supported by the limitations recited within the bodies of the independent claims.
4. Claims 2-5 and 16; 7-10 and 17-18; 12-14 and 19; and 20-21 are rejected because their dependency on rejected base Claims 1, 6, 11, and 15, respectively.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-4, 6-8, 11, and 14-21 are rejected under 35 U.S.C. 102(e)** as being anticipated by Ando (US Pub. No. 2004/0111231).
7. As to Claim 1, and similarly recited Claim 15,
testing a lot of wafers (Paragraph 0037) at two or more voltage levels (Abstract; Paragraphs 0002, 0020, 0025-0026; FIG. 2);

collecting test results (Paragraphs 0025- 0027) from the testing of the lot of wafers in a test results file (Paragraphs 0025-0027);

searching the test results file (Paragraph 0027) that contains the test results for the lot of wafers at the two or more voltage levels (Paragraphs 0025-0026); and

determining an optimal operational voltage based on test failures indicated in the results (Abstract; Paragraphs 0002, 0008, 0026-0027, 0030; FIG. 2).

8. As to Claim 2, searching the test results file comprises parsing the file (Paragraph 0027; FIG. 2).

9. As to Claim 3, searching the test results file comprises opening the file and parsing the file (Paragraphs 0020, 0023, 0027; FIG. 2).

10. As to Claim 4, determining the number of test failures at a first voltage level (Paragraphs 0025-0027); determining the number of test failures at a second voltage level (Paragraphs 0025-0027); and determining which of the first voltage level and the second voltage level had the least test failures (Paragraphs 0025-0027, 0030).

11. As to Claim 6,

a component configured to test a lot of wafers (Paragraph 0037) at two or more voltage levels (Abstract; Paragraphs 0002, 0020, 0025-0026; FIG. 2) and collect test results (Paragraphs 0025-0027) from the testing of the lot of wafers in a test results file (Paragraphs 0025-0027);

a parser module configured to search the results file (Paragraph 0027; FIG. 2) that contains test results for the lot of wafers at two or more voltage levels (Paragraphs 0025-0026);

a test failure calculation module configured to determine test failures that occurred at the two or more voltage levels (Abstract; Paragraphs 0026-0027; FIG. 2); and

a optimal operational voltage module configured to determine which of the two or more voltage levels is optimal (Paragraphs 0021, 0025-0027).

12. As to Claim 7, wherein the parser module is configured to open the test results file (Paragraphs 0020, 0023, 0027; FIG. 2).

13. As to Claim 8, wherein the parser module, the test failure calculation module, and the optimal operational voltage module comprise software that is executed by a processor (FIG. 2)

14. As to Claim 11,

logic configured to test a lot of wafers (Paragraph 0037) at two or more voltage levels (Abstract; Paragraphs 0002, 0020, 0025-0026; FIG. 2) and collect test results (Paragraphs 0025-0027) from the testing of the lot of wafers in a test results file (Paragraphs 0025-0027);

logic configured to search the test results file (Paragraph 0027; FIG. 2) that contains the test results for the lot of wafers at the two or more voltage levels (Paragraphs 0025-0026); and

logic configured to determine an optimal operational voltage based on test failures indicated in the results (Paragraphs 0021, 0025-0027).

15. As to Claim 14, determining the number of test failures at a first voltage level (Paragraphs 0025-0027); determining the number of test failures at a second voltage level (Paragraphs 0025-0027); and determining which of the first voltage level and the second voltage level had the least test failures (Paragraphs 0025-0027, 0030).

16. As to Claim 16, and similarly recited Claims 18 and 21, wherein determining an optimal operational voltage comprises determining the relative significance of the test failures (Paragraph 0027) and determining the optimal operational voltage based upon the relative significance (Abstract; Paragraphs 0002, 0008, 0026-0027, 0030).

17. As to Claim 17, and similarly recited Claims 19 and 20, wherein the optimal operational voltage module (FIG. 2) is configured to determine the number of test failures at a first voltage level (Paragraphs 0025-0027); determine the number of test failures at a second voltage level (Paragraphs 0025-0027); and determine which of the first voltage level and the second voltage level had the least test failures (Paragraphs 0025-0027, 0030).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

19. **Claims 5, 9, and 12-13 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Ando (US Pub. No. 2004/0111231) in view of Huang et al. (US Pub. No. 2003/0056029) and/or Pugh (US Pub. No. 2002/0143785).

20. Ando teaches substantially all of the limitations as stated above, except for decompressing the file in Claims 5, 9, and 12. However, Huang discloses decompressing a file (Paragraph 0050), and Pugh discloses decompressing a file (Paragraph 0033).

21. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the decompression of a file in order to:

(a) Make the file readable, since decompressing a file is well known in the art (Huang, Paragraph 0050); and/or

(b) Unzip/decompress a file for human readability is known in the art (Pugh, Paragraph 0033).

22. As to Claim 13, logic configured to search is further configured to parse the file (Ando: Paragraphs 0002, 0020, and FIG. 2).

23. **Claim 10 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Ando (US Pub. No. 2004/0111231) in view of Katla et al. (US Pub. No. 2005/0050480) and/or Wookey et al. (US Patent No. 6,182,249).

24. Ando teaches substantially all of the limitations as stated above, except for the PERL script in Claim 10. However, Katla discloses the PERL script (Paragraphs 0026 and 0052), and Wookey discloses the PERL script (Column 8, lines 4-7)

25. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the PERL script because one or more of the following:

- (a) PERL script is well known in the art for being utilized in order to implement wrapper program (Katla, Paragraph 0026); and
- (b) PERI script is well known in the art as Unix support (Katla, Paragraph 0052); and
- (c) In order to parse through the output of tests a strong processing programming language, such as PERL is utilized (Wookey, Column 8, lines 4-7).

Response to Applicant Remarks

26. The following are the applicant's remarks with respect to Ando:
- a. "Ando fails to teach testing a "lot" of wafers at two or more voltage levels or collecting test results from the testing of the lot of wafers in a test results file."
 - b. "Ando also fails to teach searching the test results file that contains the test results for the lot of wafers at the two or more voltage levels."

Examiner's Answers:

27. Ando discloses performing tests at two or more voltage levels (Paragraph 0026) on a wafer (Paragraph 0025), more specifically discloses testing a plurality of wafers (Paragraph 0037), i.e., lot; and further discloses data resulting from the test is obtained (Paragraphs 0026-0027), i.e., collected.
28. Ando discloses evaluating the results of the test (Paragraph 0027), i.e., searching, wherein the results of testing at two or more voltages is contained in test results (Paragraph 0026-0027).

Conclusion

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
30. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

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shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh Memula whose telephone number is (571) 272-8046. The examiner can normally be reached on M-F 8am-4:30pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suresh Memula

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08/18/2006


JACK CHIANG
SUPERVISORY PATENT EXAMINER